SIMULATION AND TIMING ANALYSES OF VHDL MODELS OF CODER AND DECODER OF DUOBINARY PULSE POSITION MODULATION

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ABSTRACT

Duobinary Pulse Position Modulation (DuoPPM) has been proposed as an alternative novel coding scheme which manifests many advantages over currently existing PPM formats according to the preliminary results obtained from theory and simulations run by one of the authors, Sibley. It combines the bandwidth reduction of the three-level duobinary code with the dispersion characteristics of conventional PPM. This coding is intended to be implemented using VHDL (VHSIC hardware description language) and an FPGA (Field-programmable gate array) over Plastic Optical Fibre (POF). Nevertheless if the preliminary promises of this new coding scheme are fulfilled upon successful implementation, it may be adapted to high-speed optical communications links. For the first time, the original VHDL designs, simulation results and timing analyses of DuoPPM coder and decoder are presented in this paper. These design developments are the fundamental circuits required for further investigation of this proposed coding scheme.

Keywords: Duobinary, DuoPPM, Coder, Decoder, VHDL, FPGA, Plastic optical fibre (POF)

1 INTRODUCTION

Pulse Position Modulation (PPM) schemes has been established as a leading method of utilising bandwidth available in the optical fibres, with significant improvement in sensitivity compared to equivalent Pulse Code Modulation (PCM) [1-3]. Various schemes of PPM have been proposed and investigated in the past for use in optical communications links [1-9]. Some of these PPM schemes can be attractive and suitable to implement for use in glass fibre or direct line of sight networks where bandwidth is not a concern, but unfortunately these optical communications links are expensive and not suitable for everyday use such as home networks, industrial networks and many other potentially direct consumer applications.

The authors introduce a novel coding technique that combines dibit, an alternative form of a tertiary code sometimes used in magnetic recording, and digital PPM to form DuoPPM. DuoPPM operates at only two times faster than that of the original PCM data rate, thus reducing the bandwidth, making it a potentially attractive coding scheme for Plastic Optical Fibre (POF) which suffers from low bandwidth; and high dispersion and attenuation because of the material [10-12]. Siemens AG (2007) [13] claimed to successfully achieve 1 Gbit/s data rate over POF for 100 meter long distance using Quadrature Amplitude Modulation (QAM). This claim may prove to be significant as it proves that with the rapid development in POF material and related technologies, it can achieve sufficiently high bandwidth to cater for increasingly high speed consumer demands.

PCM data coded by DuoPPM scheme is as follows: a PCM data transition from zero to zero produces a pulse in slot 0 and a one to one transition produces a pulse in slot 1 (fig 1.1). No pulses are transmitted during PCM data transitions of one to zero and zero to one and these frames are denoted as C (change). Table 1 shows the DuoPPM symbol alphabet. As there are four symbols, each symbol has a probability of $^1/_4$. However, the probability of a change sequence (C) is $^1/_2$ as it occurs with both one to zero and zero to one transitions of PCM sequence. A typical DuoPPM sequence would be 0, xC, 1 with probability of $^1/_4$, $(1/2)^x$ and $^1/_2$ respectively.

As only two slots are used to transmit one bit of PCM data, the data rate is two times that of the original PCM, thus the speed has been significantly reduced compared to digital PPM. For the first time, original VHDL hardware designs of DuoPPM coder and decoder will be presented and analysed in this paper.

2 DuoPPM CODER AND DECODER

As this is a novel coding scheme, no previous references of coder or decoder construction of such types have been found. Therefore, these circuits had to be designed, developed and implemented using VHDL and FPGA in order to carry out further investigation of the DuoPPM scheme. First of all, the circuits were designed and simulated for functional verification and functional verification does not consider FPGA delays (fan-out, inertial delay, propagation delay, gate delay etc.). All delays were considered and compensated for FPGA implementation after the functional simulations were successfully completed for both circuits. As the bit rate of the data to be coded was at a high frequency (120 Mbit/s), Altera Cyclone® II FPGA was the targeted device for the experimental implementation of the design; and timing analyses were successfully completed for the targeted device.

2.1 DuoPPM Coder

The DuoPPM coder is the part of a DuoPPM system that converts any PCM sequences into sequences that contain the DuoPPM symbols (Table 1). The PCM sequences were generated randomly by a Pseudo Random Binary Sequence (PRBS) generator. The PRBS generator was designed and implemented using VHDL language (Fig. 2.1) and the output of this PRBS block was used as the input of DuoPPM coder. The logic components that have been used to complete this DuoPPM coder are one D-type Flip-Flop (DFF), one NOR gate, 1 OR gate, one NOT gate and three AND gates. DFF delays the PCM sequence by half the clock cycle, the output of which is used with original PCM sequence to produce pulses at slots 0 and 1. Both original and delayed PCM sequences are then used as inputs to an AND gate and NOR gate. The use of clock signal and inverted clock signal are required to retime the DuoPPM pulse sequences for slot 0 and slot 1.The output of the AND gate then used as one of the two inputs of another AND gate along with the clock signal; and the output of the NOR gate is used as one of the two inputs of an AND gate along with inverted clock signal to produce pulses at slot 0 and slot 1. The outputs of the last two AND gates were then fed to the inputs of an OR gate that combines the signals to get the required DuoPPM coded sequences which have been converted from original PCM sequences.

2.2 DuoPPM Decoder

Theoretically, it is understood by engineers that a decoder could be constructed by using reverse design procedure of the coder. Nevertheless, in this case using the reverse design method produced incorrectly decoded PCM sequences because during PCM transitions of 1 to 0 and 0 to 1 no pulses were produced (Table 1). Therefore, decoding the parts of DuoPPM sequence when no pulses were available had to be carefully considered to decode the correct PCM sequence. There are two probable PCM sequences when no DuoPPM pulses were received consecutively: PCM transition of 1 to 0 and PCM transition of 0 to 1. This decision can be made if the position of the most recently received pulse, before the sequence of no pulse (C), is known. If the most recently received pulse is in slot 0 then the PCM sequence will be 1, 0, 1, 0…and so on; and if it is in slot 1 then the PCM sequence will be 0, 1, 0, 1…and so on. Therefore, a temporary memory block had to be designed using D-Type Flip-flops (DFF) and logic gates to store the most recently received DuoPPM pulse position. The logic components that have been used to complete the DuoPPM decoder are 12 DFFs, 6 XOR gates, 2 NOT gates, 1 XNOR gate, 2 NAND gates and 8 AND gates. The complexity of the decoder design increased due to be able to correctly decode PCM sequences when there were no pulses (C) received in DuoPPM sequence.

3 SIMULATION RESULTS OF CODER AND DECODER

3.1 Simulation Results of DuoPPM Coder

Running the system with PRBS sequences as PCM input sequence is shown in figure 3.1 operating at 120MHz clock frequency. As it can be observed (fig 3.1) that the coded DuoPPM sequence for the input PCM sequence (PRBS) was as expected (table 1) according to the theory of this coding scheme. Figure 3.1 clearly demonstrates that consecutive PCM bits of 1 produce pulses at slot 1 of the DuoPPM frame at the beginning of the second half of a clock period and consecutive PCM bits of 0 produce pulses at slot 0 of the DuoPPM frame at the beginning of a clock period for half a clock cycle.

3.2 Simulation Results of DuoPPM Decoder

Designed decoder of the system was tested by operating at the same frequency as the coder, 120MHz. Input DuoPPM sequences were taken from the output of the coder and the final decoded PCM sequence was compared with the input PCM (PRBS) sequence of the coder for functional verification of the decoder. Simulation result of the decoded output waveform is shown in figure 3.2. As expected the start edge of every decoded PCM pulse starts when the clock period starts. Figure 3.3 shows the simulation result of the complete system (coder and decoder) where coded DuoPPM is used as input of the decoder and the decoded PCM sequence can be observed. From the comparison of the PCM input sequence of the coder and the decoded PCM output sequence of the decoder it can be seen that the DuoPPM sequence has been correctly decoded back to PCM sequence. The short delay that appears between these two sequences is a result of the DFF delay in the decoder. Further checks were carried out to confirm the validity of the decoder output by using an XOR gate as Bit Error Rate Test (BERT) device. Both coder input PCM sequence and decoder PCM output sequence were synchronised and used as inputs of the XOR gate and no errors were registered.

4 TIMING ANALYSES OF CODER AND DECODER

4.1 Timing Analyses of DuoPPM Coder and Decoder

In order to practically implement the designed coder and decoder on an FPGA timing analysis on all logic circuits needed to be completed since functional simulation does not consider any timing delays. First of all, the delays were identified for both circuits and required measures had to be taken to either remove the delays or if they were not removable then measures had to be taken to compensate for the existing delays as the signals need to be synchronised with the clock signals to produce correct outputs. Main types of delays identified for the circuits were inertia delay which is inherent in FPGA, transport delay (propagation delay), gate delays, fan-out and clock skew. Most of the delays were compensated by using DFFs that produce more delay to make the signals synchronised with required signals. The delays in coder circuit were compensated using additional logic elements of 3 DFFs, 1 OR gate and 1 NOR gate. Existing delays in the decoder circuit were compensated with the use of 19 additional DFFs. For functional simulation, 120MHz clock was used which is the frequency for PCM. But for practical timing analysis it was determined that two different clock frequencies were required: one 240MHz clock for DuoPPM as it runs at the data rate two times that of PCM thus PCM requires a 120MHz clock. Phase-locked Loop (PLL) was used to process the external 240MHz clock signal and it produces two output clock signals of 120MHz and 240MHz; and both output clock signals were source synchronised. The clock signals had to available throughout both circuits as dedicated clock signals to avoid any delays related to clock skew. Therefore, the clock signals were routed in the circuits as GLOBAL signals available approximately at the same time at different components minimising the effects of clock skew. If the clock signals are not routed as GLOBAL signals then FPGA will consider them as general signals and this may cause, in synchronous circuits, the signals to arrive at different components at different times causing erroneous outputs from logic components.

4.2 Timing Analyses Measurements of DuoPPM Coder and Decoder

Figure 4.1 shows the complete circuit block schematic after design analyses were completed and input/output pins were assigned which will be implemented on FPGA. As it can be seen, a PLL circuit block was added for clock division and source synchronisation of the clock signals. This PLL can also be used during further investigation of slot and frame synchronisation and clock extraction for the received DuoPPM sequence. An MLSD error detector and corrector was also constructed using an original algorithm for this coding scheme which can also be seen from figure 4.1. As it can be observed from the timing analysis output waveform in figure 4.2 that the PLL, coder, decoder and MLSD error detector and corrector produces correct results at each stage of the circuit by compensating or removing all types of delays. It is also noticeable from figure 4.1 that there is delay of approximately 217ns from received DuoPPM sequence to the decoded PCM sequence. Most of this delay is due to MLSD error detector and corrector’s register buffer and the rest is due to the delay compensation in the decoder.

5 CONCLUSIONS

The design and development of DuoPPM coder and decoder have been presented in this paper for the first time. Theoretical representations of DuoPPM coder and decoder waveforms and VHDL design simulation outputs haven shown. Two fundamental and essential parts of the system, coder and decoder, have been developed and further investigation on DuoPPM scheme can be carried out using these circuits.

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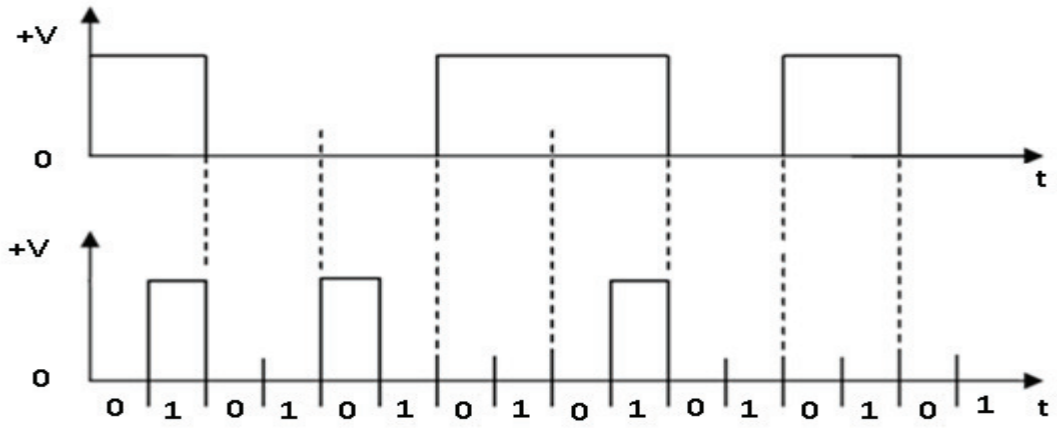

Fig. 1.1: Conversion of PCM data (top trace) to DuoPPM (bottom trace).

PCM	Probability	DuoPPM	Symbol
00	1/4	Pulse in slot 0	0
01	1/4	No pulse	C
10	1/4	No pulse	C
11	1/4	Pulse in slot 1	1

Table 1: DuoPPM symbol alphabet.

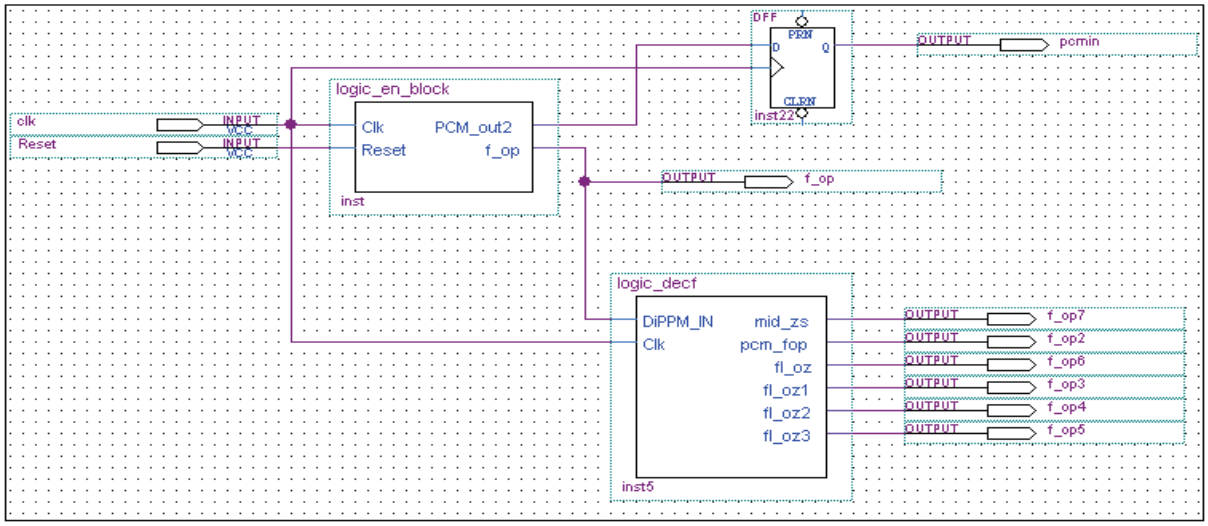

Fig. 2.1: VHDL coder and decoder block diagram schematic of DuoPPM decoder circuit.

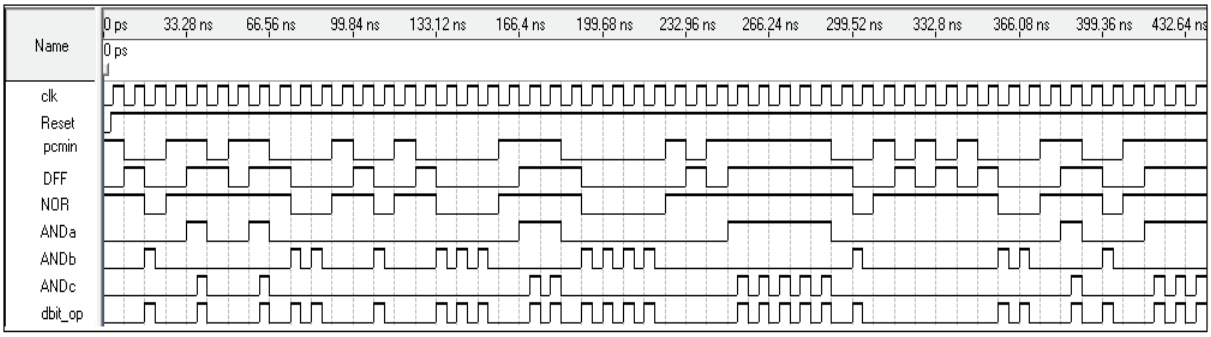

Fig. 3.1: VHDL coder simulation output waveform.

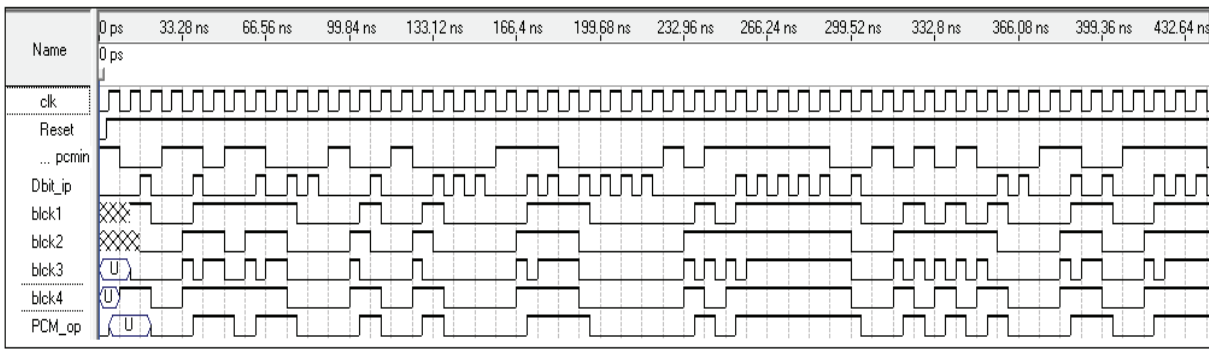

Fig. 3.2: VHDL decoder simulation output waveform.

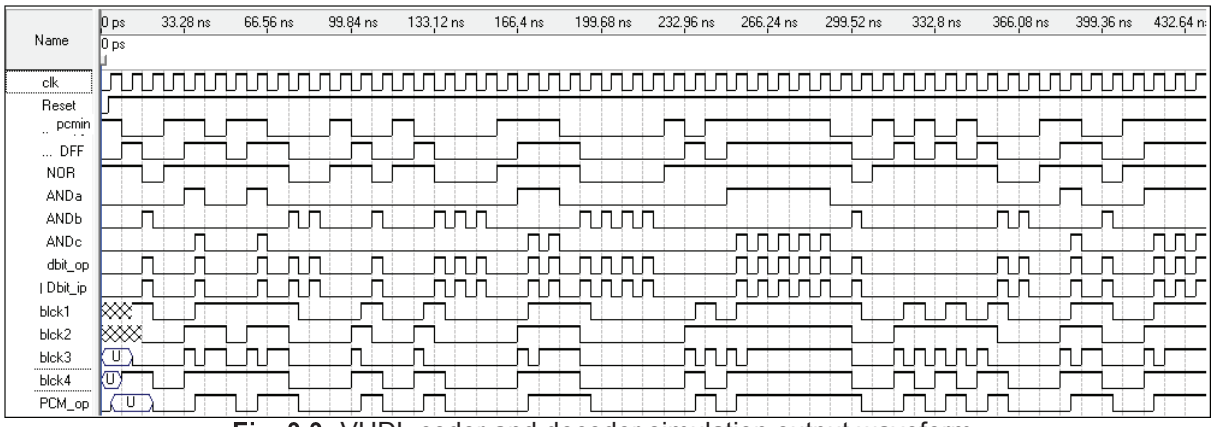

Fig. 3.3: VHDL coder and decoder simulation output waveform.

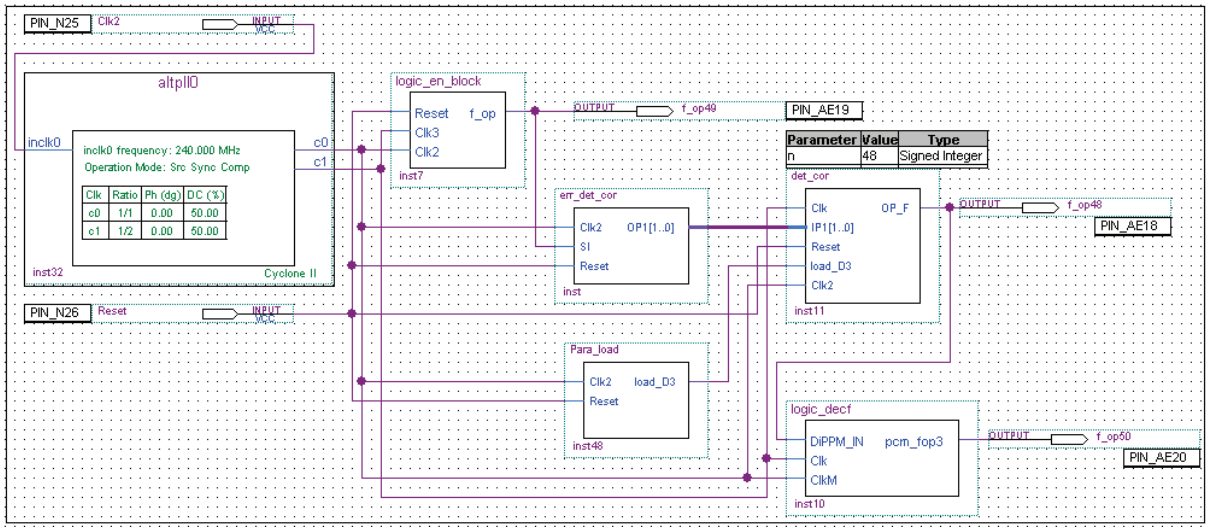

Fig. 4.1: Complete DuoPPM system after timing analysis (coder, decoder and MLSD error detector).

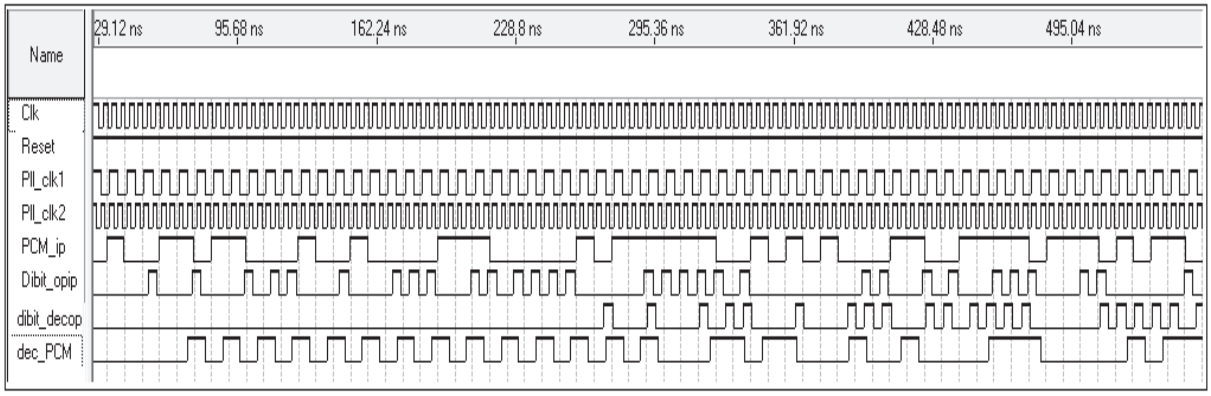

Fig. 4.2: Complete DuoPPM system timing analysis output waveform (coder and decoder).